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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/320,421	05/26/99	FORBES L	303.586US1

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EXAMINER	
TRA, A	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/21/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/320,421	Applicant(s) Forbes
	Examiner Anh-Quan Tra	Group Art Unit 2816

☒ Responsive to communication(s) filed on *May 26, 1999* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-45* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-45* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *May 26, 1999* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the dual-gated transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-16, 29-39, 44, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawashima (U.S. Patent No. 5699305).

As to claims 1, 10, 33, 35, 36, 37, Kawashima discloses in figure 7 a sense amplifier (105) comprising: a pair of cross-coupled inverters (66-69, and 72-75), wherein each inverter includes: a transistor of a first conductivity type (66, 67), a pair of transistors of second conductivity type (68, 69, 74, 75) coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type; a pair of bit lines (IN, /IN), wherein each one of the pair of bit lines is coupled

to a gate of a first one of the pair of transistors in each inverter; and a pair of output transmission lines (OUT, /OUT), wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

As to claims 2, 4, 11, 34, and 38, figure 7 discloses the transistor of first conductivity type is a p-channel metal oxide semiconductor transistor, and the pair of transistors of second conductivity type are n-channel metal oxide semiconductor transistors.

As to claims 29 and 32, figure 1 shows an SRAM circuit comprising a sense amplifier 29. It is inherent that the SRAM circuit is connected to a processor.

As to claims 3, 5, 12, and 39, the drain region for NMOS transistors and the drain region for the PMOS transistor in one inverter is further coupled to the gates of the PMOS transistor and a second one of the NMOS transistors in the other inverter.

As to claims 6, 13, 44, and 45, the bit line capacitances are removed from the pair of output transmission lines.

As called for claims 7 and 14, figure 1 shows that the sense amplifier circuit (29) is coupled to a number of memory cells (1-9) in an array of memory cells.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

4. Claims 1-16, 29-39, 44, and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Austin (U.S. Patent No. 5982690).

As to claims 1, 10, 33, 35, 36, 37, Austin discloses in figure 1D a sense amplifier (105) comprising: a pair of cross-coupled inverters (153, 155 and 154, 156), wherein each inverter includes: a transistor of a first conductivity type (P5, P6), a pair of transistors of second conductivity type (N5, N6, N7, N8) coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type; a pair of bit lines (output of 103), wherein each one of the pair of bit lines is coupled to a gate of a first one of the pair of transistors in each inverter; and a pair of output transmission lines (lat, /lat), wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

As to claims 2, 4, 11, 34, and 38, figure 1D discloses the transistor of first conductivity type is a p-channel metal oxide semiconductor transistor, and the pair of transistors of second conductivity type are n-channel metal oxide semiconductor transistors.

As to claims 29 and 32, figure 4 discloses a processor (473); a memory device (470).

As to claims 3, 5, 12, and 39, the drain region for NMOS transistors and the drain region for the PMOS transistor in one inverter is further coupled to the gates of the PMOS transistor and a second one of the NMOS transistors in the other inverter.

As to claims 6, 13, 44, and 45, the bit line capacitances are removed from the pair of output transmission lines.

As called for claims 7 and 14, figure 5 shows that the sense amplifier circuit (200) is coupled to the memory cell (500), it is inherent that the RAM (470) comprises plurality of memory cells.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8, 9,15-22, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin (U.S. Patent No. 5982690).

As to claims 8, 9, 15, 16, 30, and 31, Austin's figure 1D shows all elements of the claimed invention except that it does not show the value of the supply voltage is less than 1.0 Volts and the output delay times is less than 10 ns. However, the selection of the supply voltage value to be less than 1.0 Volts and the output delay times to be less than 10 ns is seen as an obvious design expedient dependent upon the particular environment of use to ensure optimum performance.

Austin's figure 1D shows all elements of the claimed invention except that it does not show the dual-gated MOSFET transistors included in the first and second inverters. However, it

would have been obvious to one having an ordinary skill in the art to replace the pairs of transistors (153 and 154) with the dual-gated MOSFET transistors for the purpose of saving space.

7. Claims 23-28 and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (U.S. Patent No. 6069828) in view of Austin (U.S. Patent No. 5982690).

As to claim 23, Kaneko et al. teaches in figure 2 a memory circuit comprising a number of memory arrays (two sides of sense amplifier 15); a sense amplifier (15), a complementary pair of bit lines (BL1, /BL1, BL2, /BL2) input to the sense amplifier. Thus, figure 2 shows all elements of the claim except that it does not show the sense amplifier comprising a pair of cross-coupled inverters, wherein each inverter includes a pair of parallel n-channel transistor coupled in series with a p-channel transistor. However, Austin shows in figure 1D a sense amplifier circuit (105) comprising a pair of cross-coupled inverters (153, 155 and 154, 156), wherein each inverter includes: a PMOS transistor (P5, P6), a pair of NMOS transistors (N5, N6, N7, N8) coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of NMOS transistors is coupled to a drain region of the PMOS transistor; a pair of bit lines (output of 103), wherein each one of the pair of bit lines is coupled to a gate of a first one of the pair of NMOS transistors in each inverter; and a pair of output transmission lines (lat, /lat), wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of NMOS transistors and the drain region of the PMOS transistor in each inverter for the purpose of saving power consumption. Therefore, it would have been obvious to one having an ordinary skill in the art to

use the sense amplifier circuit of Austin into the sense amplifier (15) of Kaneko et al.'s figure 2 for the purpose of saving power consumption.

As to claim 24, Austin's figure 1D shows that the memory circuit includes a folded bit line.

As to claims 25, the drain region for NMOS transistors and the drain region for the PMOS transistor in one inverter is further coupled to the gates of the PMOS transistor and a second one of the NMOS transistors in the other inverter.

As to claims 28 and 40, Kaneko et al.'s figure 2 shows number of equilibration (14a, b) and a number of isolation (18a, b) transistors coupled to the complementary pair of bit lines.

As to claims 26, 27, 41, and 42, the selection of the supply voltage value to be less than 1.0 Volts and the output delay times to be less than 10 ns is seen as an obvious design expedient dependent upon the particular environment of use to ensure optimum performance.

As to claim 43, Austin's figure 1D shows a step of removing the bit line capacitance from the output nodes.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is (703) 308-6174. The examiner can normally be reached on Monday to Friday from 7:40 am to 4:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reach at (703) 308-4876. The fax phone number for this group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

QT

June 17, 2000

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